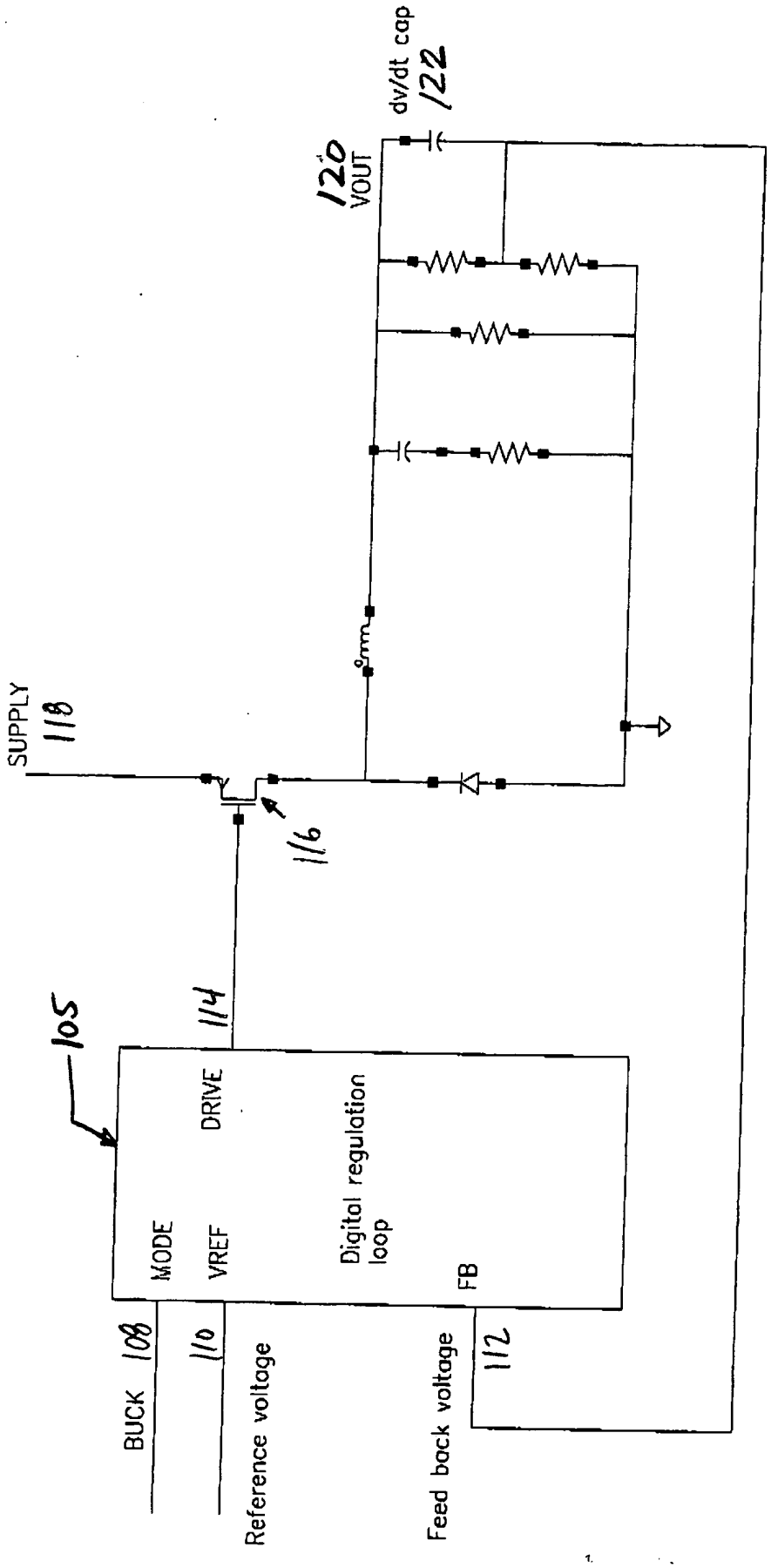
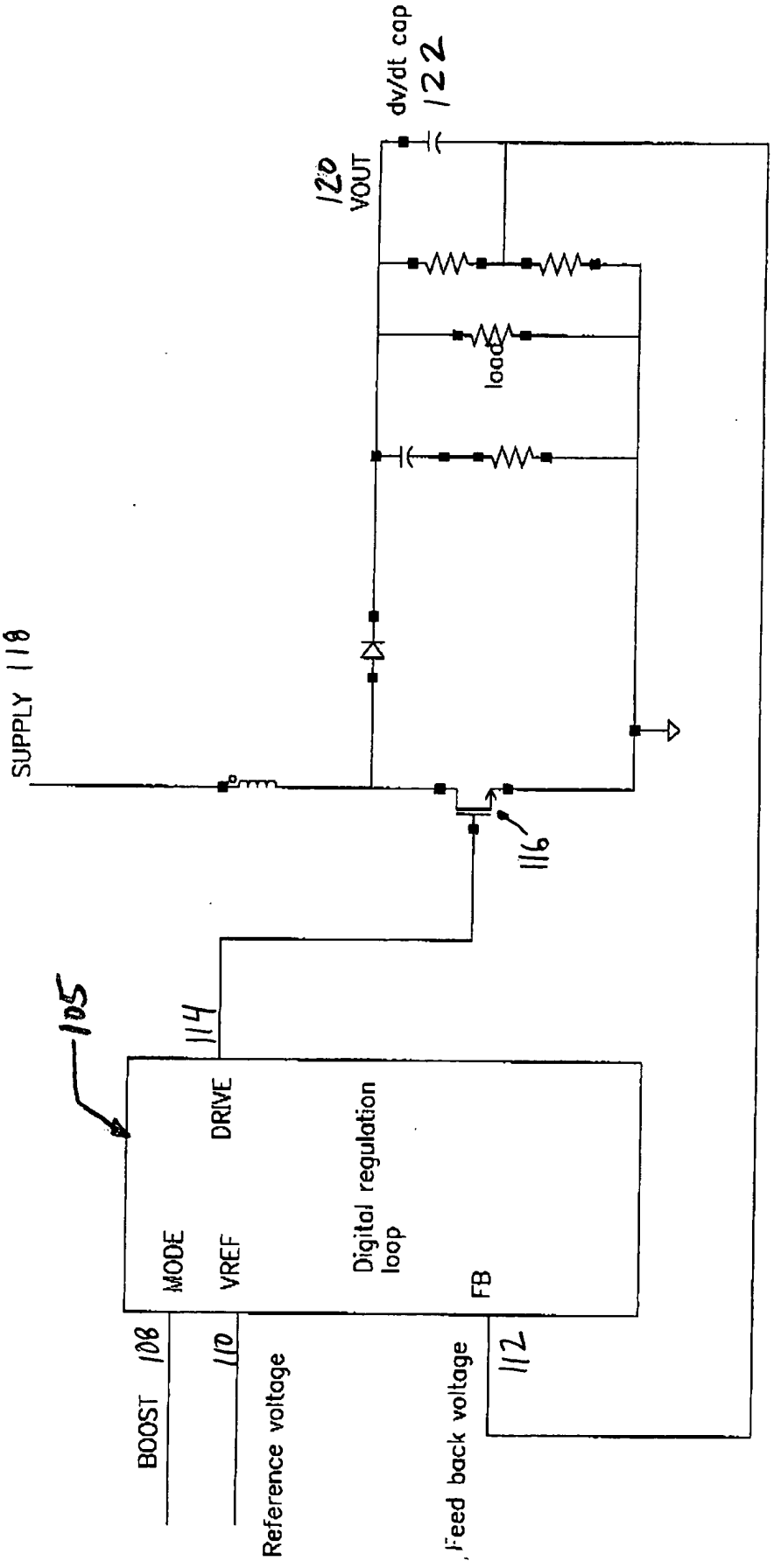


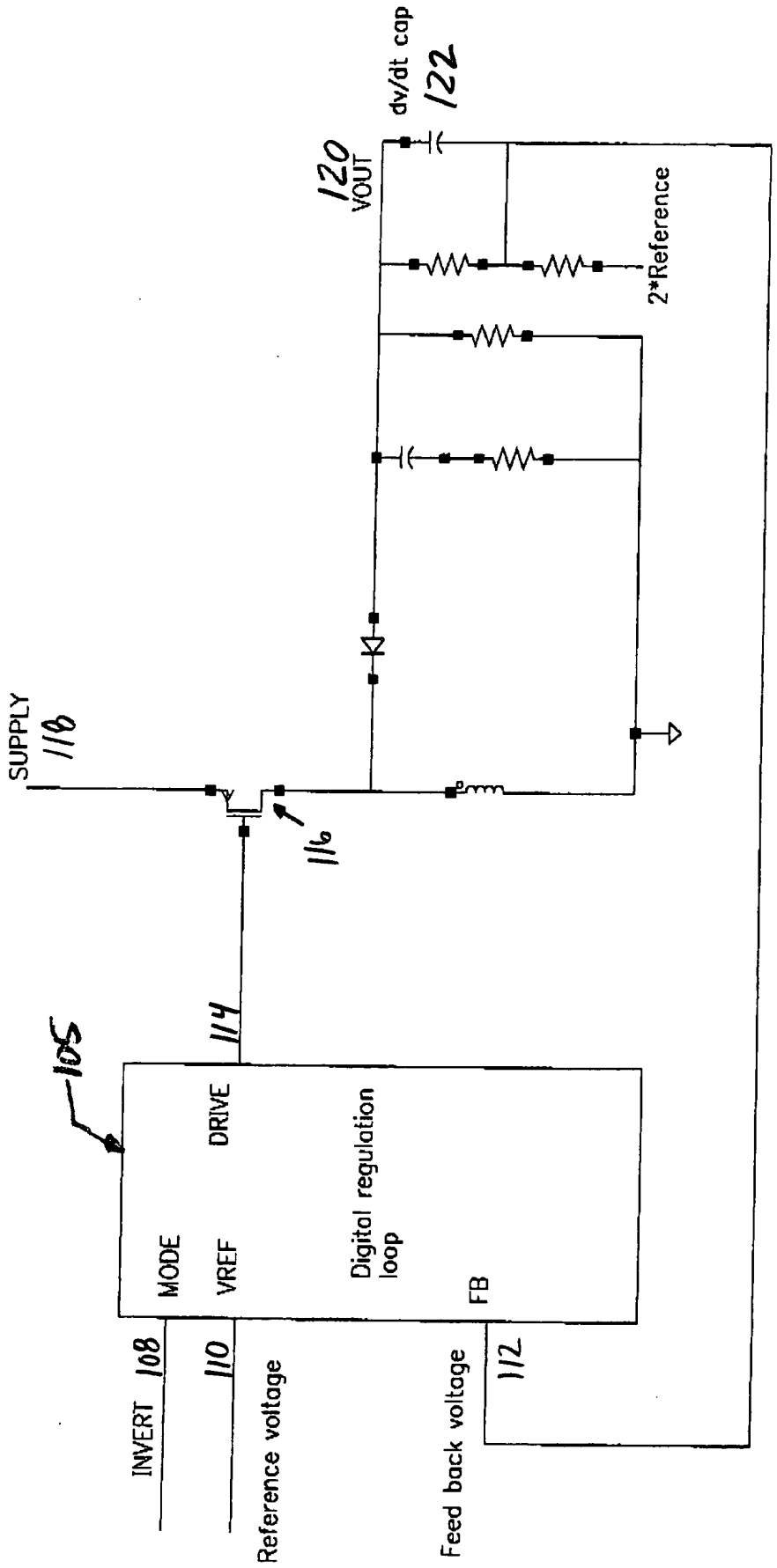
Digital regulation loop configured in Buck mode

FIG. 1A



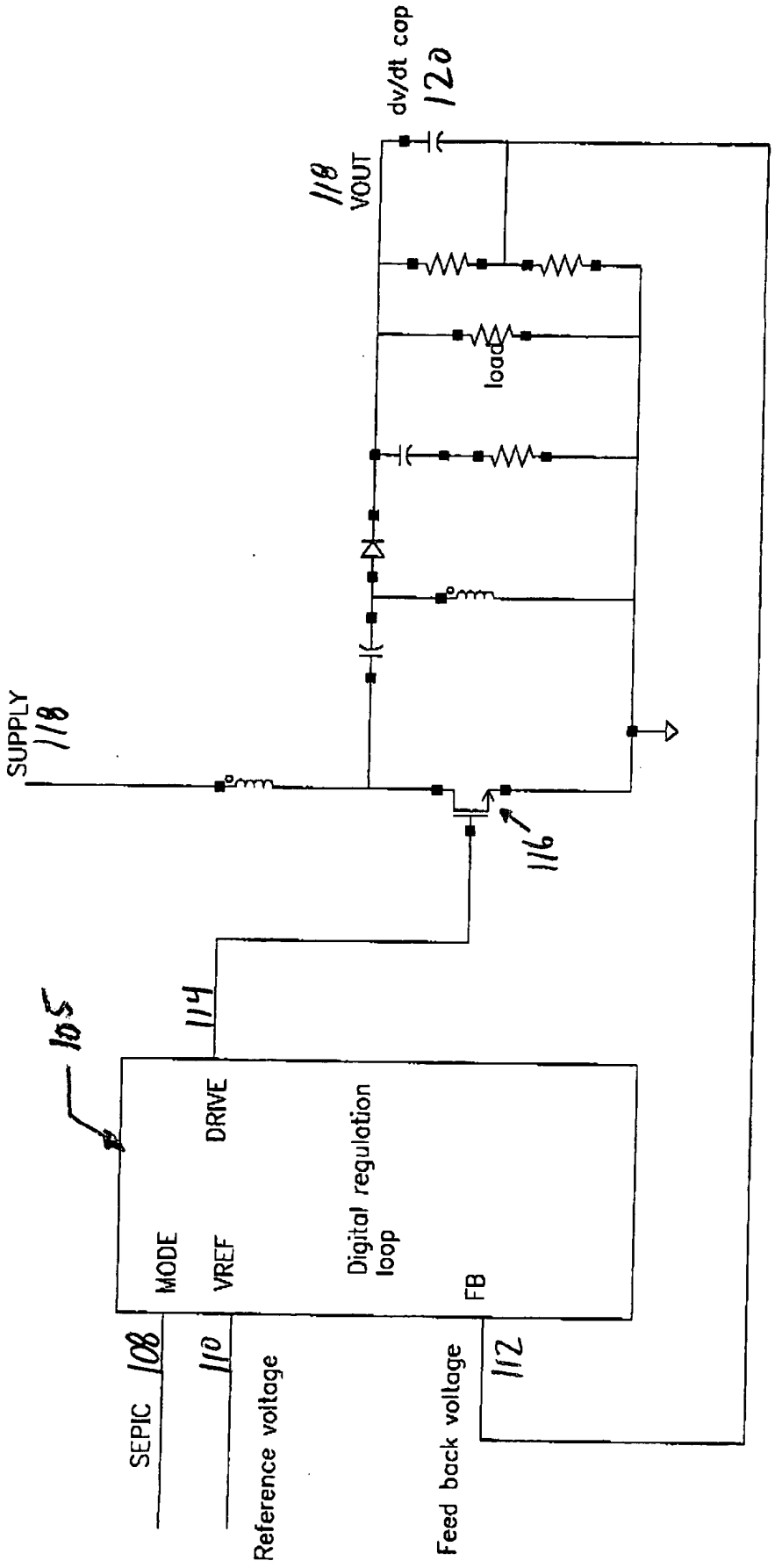
Digital regulation loop configured in BOOST mode

FIG. 1B



Digital regulation loop configured in inverter mode

FIG. 1C



Digital regulation loop configured in SEPIC mode

FIG. 1D

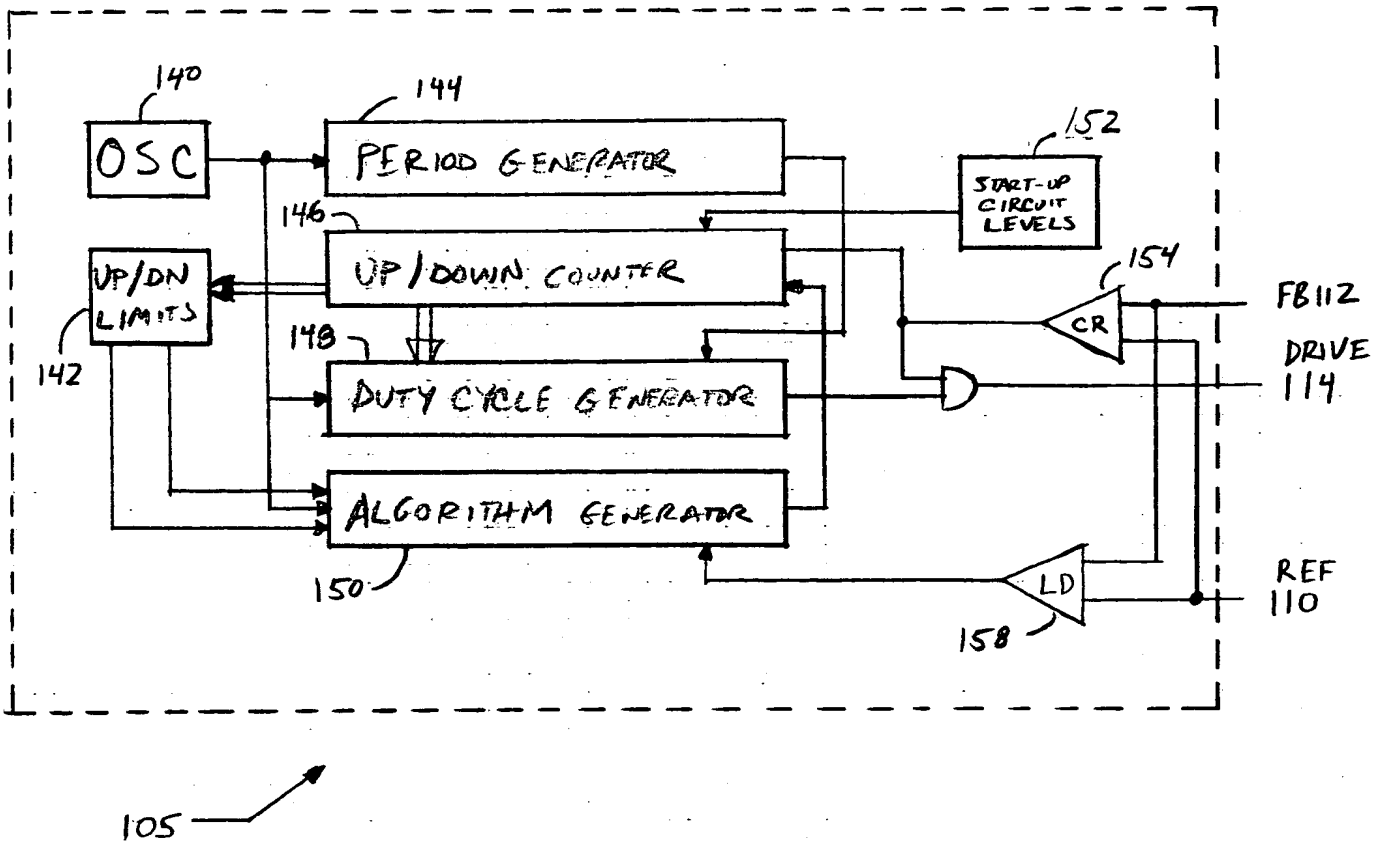

140
OSC
144
PERIOD GENERATOR
152
START-UP CIRCUIT LEVELS
146
UP/DOWN COUNTER
UP/DN LIMITS
142
154
CR
FB 112
148
DUTY CYCLE GENERATOR
DRIVE 114
ALGORITHM GENERATOR
150
LD
158
REF 110
105

FIG. 2

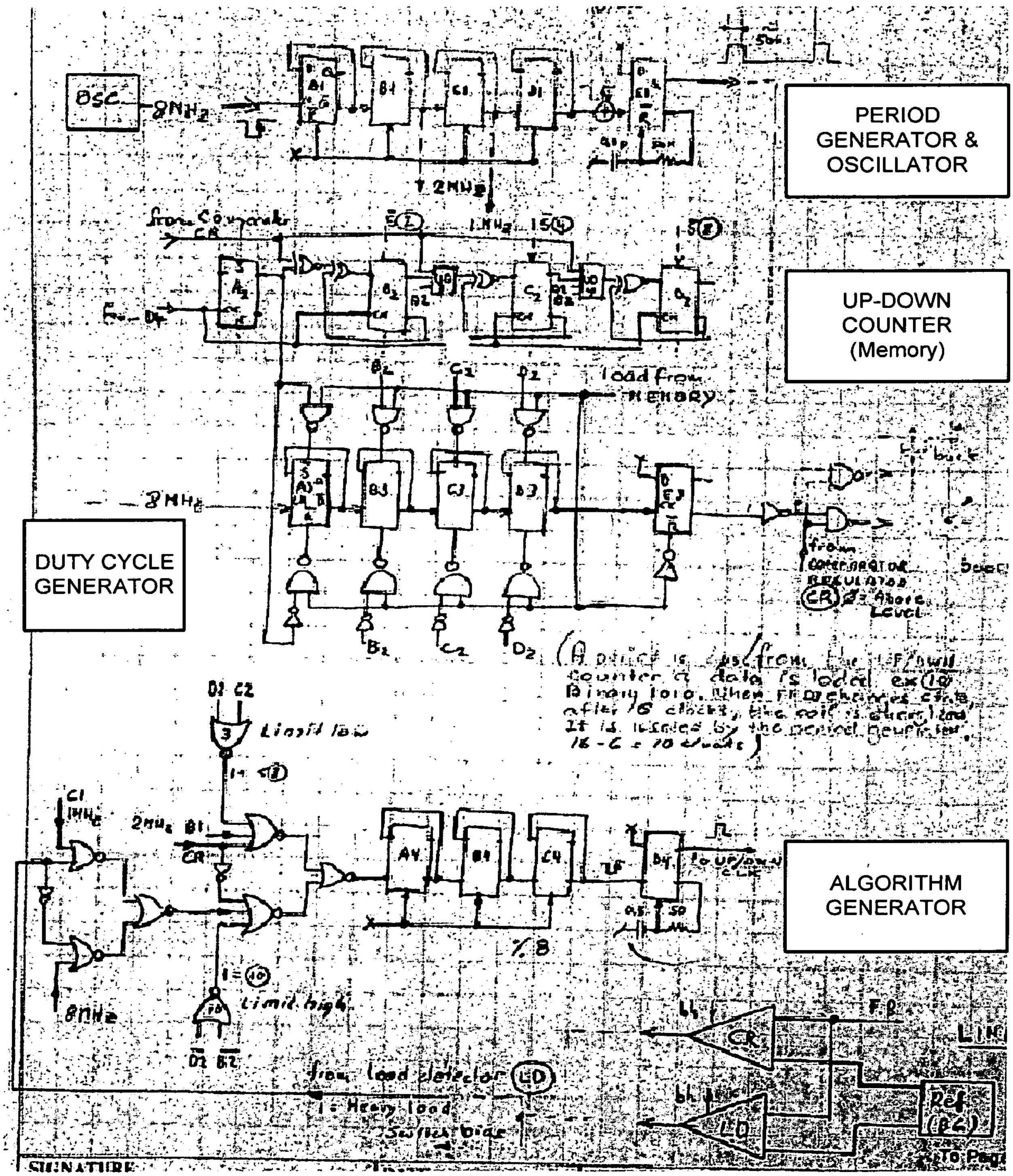

PERIOD GENERATOR & OSCILLATOR
UP-DOWN COUNTER (Memory)
DUTY CYCLE GENERATOR
ALGORITHM GENERATOR
OSC
8MHz
2MHz
1MHz
load from MEMORY
from load detector
1 = Heavy load
limit low
limit high
÷8
Ref
CR
LD

FIG. 3

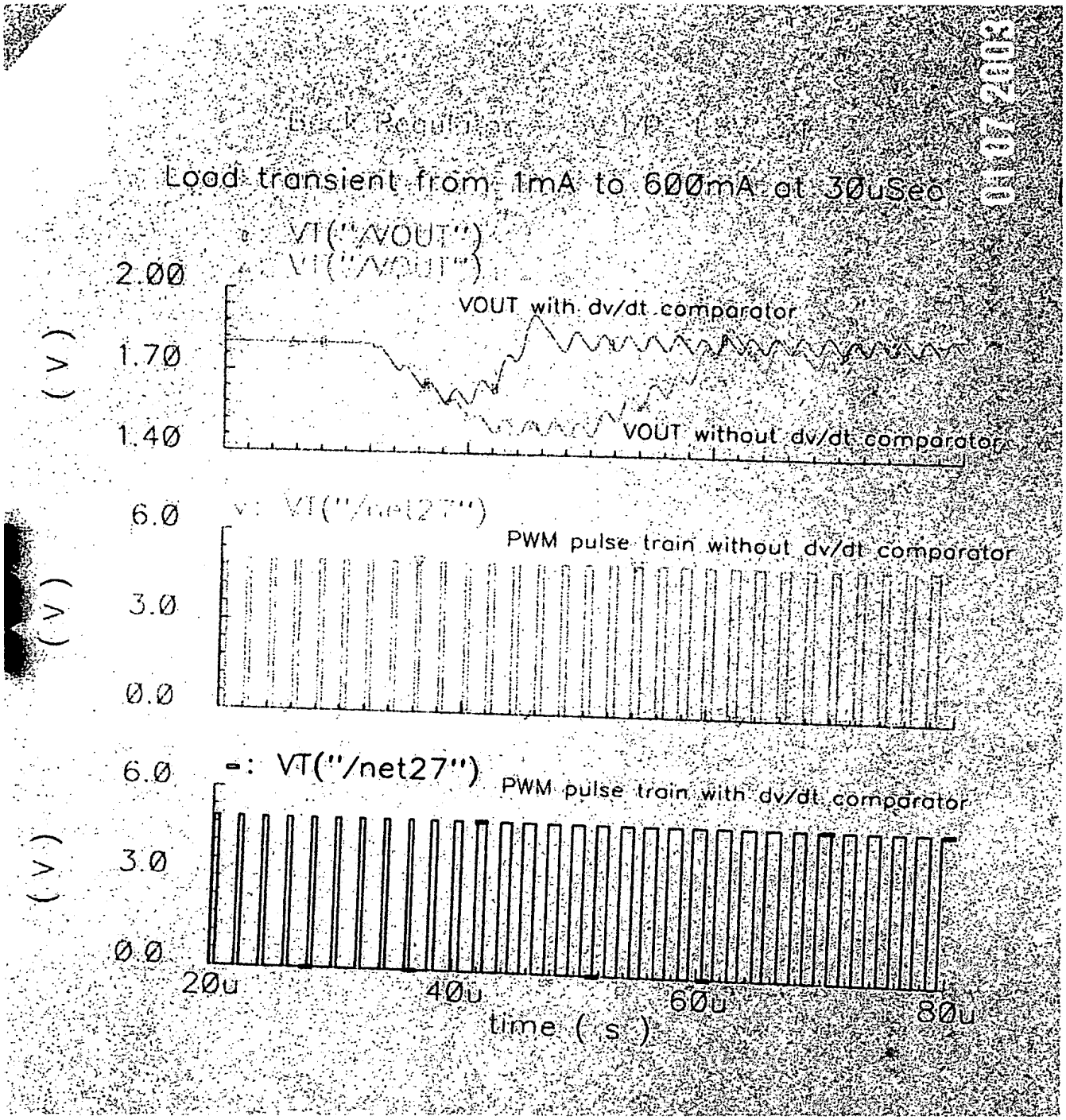

Load transient from 1mA to 600mA at 30uSec
V(/VOUT)
2.00
1.70
1.40
(V)
VOUT with dv/dt comparator
VOUT without dv/dt comparator
6.0
3.0
0.0
(V)
PWM pulse train without dv/dt comparator
6.0
3.0
0.0
(V)
V(/net27)
PWM pulse train with dv/dt comparator
20u
40u
60u
80u
time (s)

FIG. 4

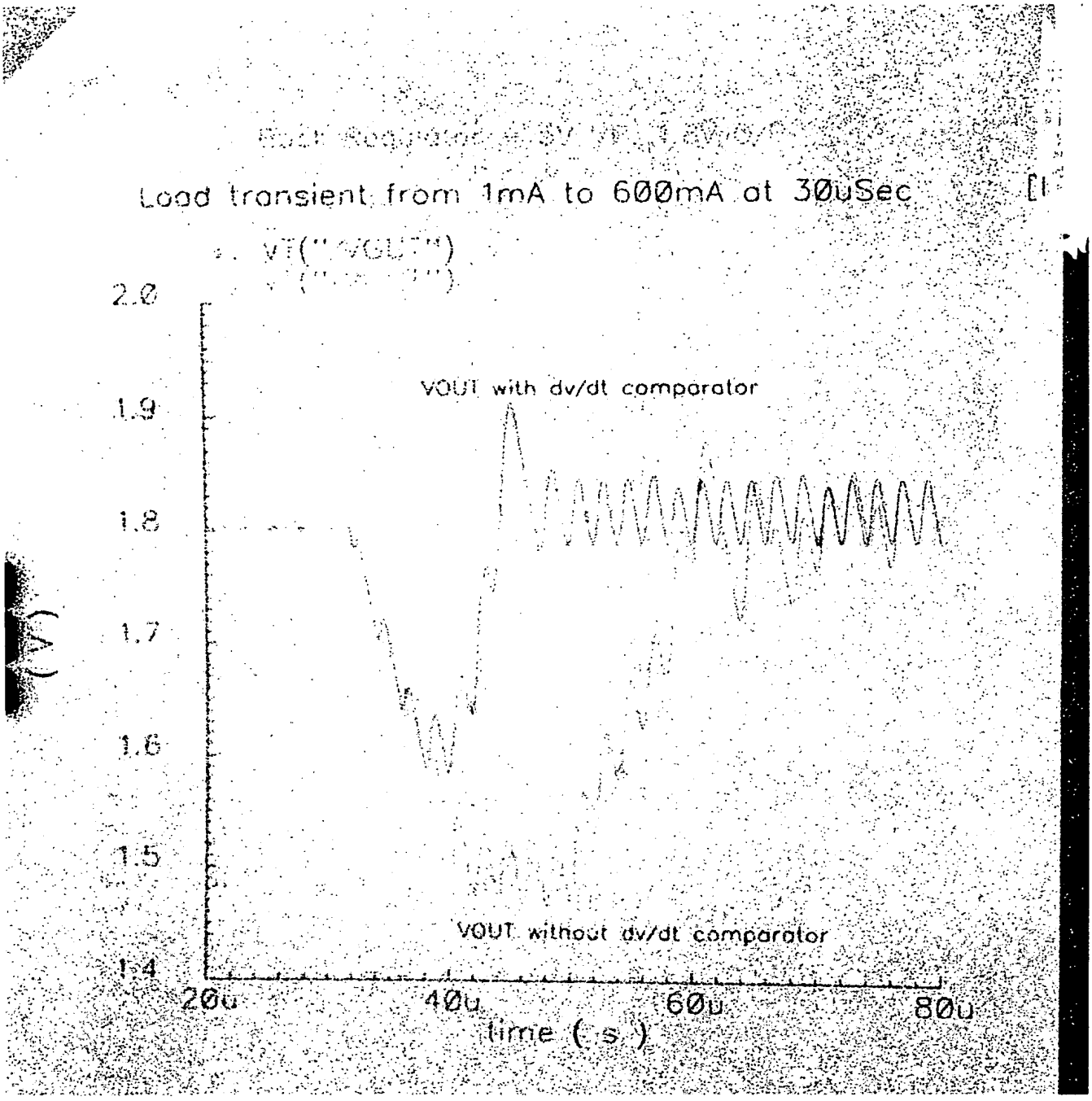

Load transient from 1mA to 600mA at 30uSec
VT("VOUT")
2.0
1.9
1.8
1.7
1.6
1.5
1.4
VOUT with dv/dt comparator
VOUT without dv/dt comparator
20u
40u
60u
80u
Time (s)

FIG. 5